ANALOG FRONT-END HAVING BUILT-IN EQUALIZATION AND APPLICATIONS THEREOF

BACKGROUND OF THE INVENTION

TECHNICAL FIELD OF THE INVENTION

[0001] This invention relates generally to communication systems and more particularly to an enhanced data conveyance within such communication systems.

DESCRIPTION OF RELATED ART

[0002] Communication systems are known to transport large amounts of data between a plurality of end user devices. Such end user devices include telephones, facsimile machines, computers, television sets, cellular phones, personal digital assistants, et cetera. As is also known, such communication systems may be a local area network (LAN) and/or a wide area network (WAN). A local area network is generally understood to be a network that interconnects a plurality of end user devices distributed over a localized area (e.g., up to a radius of 10 kilometers) and includes LAN infrastructure equipment. For example, a local area network may be used to interconnect workstations distributed within an office of a single building or a group of buildings, to interconnect computer based equipment distributed around a factory or As is further known, local area hospital, et cetera. networks may be wired local area networks or wireless local area networks. Wired local area networks typically have a star topology, ring topology, bus topology or hub/tree topology.

[0003] A wide area network is generally understood to be a network that covers a wide geographic area and includes WAN infrastructure equipment. Wide area networks include both public data networks and enterprise wide private data networks. A public data network is established and operated by a national network administrator specifically for data transmission. Such public data networks facilitate the inner

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The receiver of many standardized protocols.

[0009] Therefore, a need exists for programmable equalizer for use within receiver sections of high-speed data interfaces.

BRIEF SUMMARY OF THE INVENTION

[0010] The analog front-end having built-in equalization of the present invention substantially meets these needs and In one embodiment, an analog front-end having builtin equalization includes a control module and a tunable gain The control module is operably coupled to provide a frequency response setting based on a channel response of a channel providing high-speed serial data to the analog front-The tunable gain stage includes a frequency dependent end. load and an amplifier input section. The frequency dependent load is adjusted based on the frequency response setting. The amplifier input section is operably coupled to the frequency dependent load and receives the high-speed serial In conjunction with the frequency dependent load, the data. amplifier input section amplifies and equalizes the highspeed serial data to produce an amplified and equalized serial data. As such, an analog front-end may have its built-in equalizer adjusted to compensate for the varying channel responses.

[0011] In another embodiment, an analog front-end having built-in equalization includes a frequency dependent load, and amplifier input section. The amplifier input section is operably coupled to the frequency dependent load and receives high-speed serial data. In conjunction with the frequency dependent load, the amplifier input section amplifies and equalizes the high-speed serial data to produce an amplified and equalized serial data.

[0012] Such an analog front-end having built-in equalization may be incorporated in a high-speed data receiver that receives high-speed serial data via a channel. The channel may be of varying lengths and as such have varying channel responses. Based on the channel response,

the analog front-end is adjusted to provide an appropriate level of equalization.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

- [0013] Figure 1 is a schematic block diagram of a programmable logic device in accordance with the present invention;
- [0014] Figure 2 is a schematic block diagram of a programmable multi-gigabit transceiver in accordance with the present invention;
- [0015] Figure 3 is a schematic block diagram of a programmable receive physical media attachment (PMA) module in accordance with the present invention;
- [0016] Figure 4 is a schematic block diagram of a programmable front-end in accordance with the present invention;
- [0017] Figure 5 is a schematic block diagram of an alternate embodiment of a programmable front-end in accordance with the present invention;
- [0018] Figures 6 and 6A are schematic block diagrams of various embodiments of a tunable gain stage in accordance with the present invention;
- [0019] Figure 7 is a schematic block diagram of an alternate embodiment of a tunable gain stage in accordance with the present invention; and
- [0020] Figures 8A-8D illustrate various channels, channel responses and programmable equalization in accordance with the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0021] Figure 1 is a schematic block diagram of a programmable logic device 10 that includes programmable logic fabric 12, a plurality of programmable multi-gigabit transceivers (PMGT) 14-28 and a control module 30. The programmable logic device 10 may be a programmable logic

array device, a programmable array logic device, an erasable programmable logic device, and/or a field programmable gate array (FPGA). When the programmable logic device 10 is a field programmable gate array (FPGA), the programmable logic fabric 12 may be implemented as a symmetric array configuration, a row-based configuration, a sea-of-gates configuration, and/or a hierarchical programmable logic device configuration. The programmable logic fabric 12 may further include at least one dedicated fixed processor, such as a microprocessor core, to further facilitate the programmable flexibility offered by a programmable logic device 10.

The control module 30 may be contained within the [0022] programmable logic fabric 12 or it may be a separate module. In either implementation, the control module 30 generates the control signals to program each of the transmit and receive sections of the programmable multi-gigabit transceivers 14-In general, each of the programmable multi-gigabit 28. transceivers 14-28 performs a serial-to-parallel conversion on received data and performs a parallel-to-serial conversion on transmit data. The parallel data may be 8-bits, 16-bits, 32-bits, 64-bits, et cetera wide. Typically, the serial data will be a 1-bit stream of data that may be a binary level signal, multi-level signal, etc. Further, two or more programmable multi-gigabit transceivers may be bonded together to provide greater transmitting speeds. For example, if multi-gigabit transceivers 14, 16 and 18 are transceiving data at 3.125 gigabits-per-second, the transceivers 14-18 may be bonded together such that the effective serial rate is 3 times 3.125 gigabits-per-second.

[0023] Each of the programmable multi-gigabit transceivers 14-28 may be individually programmed to conform to separate standards. In addition, the transmit path and receive path of each multi-gigabit transceiver 14-28 may be separately programmed such that the transmit path of a transceiver is supporting one standard while the receive path of the same

transceiver is supporting a different standard. Further, the serial rates of the transmit path and receive path may be programmed from 1 gigabit-per-second to tens of gigabits-per-second. The size of the parallel data in the transmit and receive sections, or paths, is also programmable and may vary from 8-bits, 16-bits, 32-bits, 64-bits, et cetera.

Figure 2 is a schematic block diagram of one [0024] embodiment of a representative one of the programmable multigigabit transceivers 14-28. As shown, the programmable multi-gigabit transceiver includes a programmable physical media attachment (PMA) module 32, a programmable physical coding sub-layer (PCS) module 34, a programmable interface 36, a control module 35, a PMA memory mapping register 45 and a PCS register 56. The control module 35, based on the desired mode of operation for the individual programmable multi-gigabit transceiver 14-28, generates a programmed deserialization setting 66, a programmed serialization setting 64, a receive PMA_PCS interface setting 62, a transmit PMA_PCS interface setting 60, and a logic interface setting 58. The control module 35 may be a separate device within each of the multi-gigabit transceivers and/or included within the control module 30. In either embodiment of the PMGT control module 35, the programmable logic device control module 30 determines the corresponding overall desired operating conditions for the programmable logic device 10 and provides the corresponding operating parameters for a given multi-gigabit transceiver to its control module 35, which generates the settings 58-66.

[0025] The programmable physical media attachment (PMA) module 32 includes a programmable transmit PMA module 38 and a programmable receive PMA module 40. The programmable transmit PMA module 38 is operably coupled to convert transmit parallel data 48 into transmit serial data 50 in accordance with the programmed serialization setting 64. The programmed serialization setting 64 indicates the desired rate of the transmit serial data 50, the desired rate of the

transmit parallel data 48, and the data width of the transmit parallel data 48. The programmable receive PMA module 40, which will be described in greater detail with reference to Figure 3, is operably coupled to convert receive serial data 52 into receive parallel data 54 based on the programmed describilization setting 66. The programmed describilization setting 66 indicates the rate of the receive serial data 52, the desired rate of the receive parallel data 54, and the data width of the receive parallel data 54. The PMA memory mapping register 45 may store the serialization setting 64 and the describilization setting 66.

The programmable physical coding sub-layer (PCS) module 34 includes a programmable transmit PCS module 42 and a programmable receive PCS module 44. The programmable transmit PCS module 42 receives transmit data words 46 from the programmable logic fabric 12 via the programmable interface 36 and converts them into the transmit parallel data 48 in accordance with the transmit PMA PCS interface setting 60. The transmit PMA PCS interface setting 60 indicates the rate of the transmit data words 46, the size of the transmit data words (e.g., 1-byte, 2-bytes, 3-bytes, 4bytes, et cetera) and the corresponding transmission rate of the transmit parallel data 48. The programmable receive PCS module 44 converts the received parallel data 54 into received data words 56 in accordance with the receive PMA PCS interface setting 62. The received PMA PCS interface setting 62 indicates the rate at which the received parallel data 54 will be received, the width of the parallel data 54, the transmit rate of the received data words 56 and the word size of the received data words 56.

[0027] The control module 35 also generates the logic interface setting 58 that provides the rates at which the transmit data words 46 and receive data words 56 will be transceived with the programmable logic fabric 12. Note that the transmit data words 46 may be received from the programmable logic fabric 12 at a different rate than the

received data words 56 are provided to the programmable logic fabric 12.

[0028] As one of average skill in the art will appreciate, each of the modules within the PMA module 32 and PCS module 34 may be individually programmed to support a desired data transfer rate. The data transfer rate may be in accordance with a particular standard, such that the receive path, i.e., the programmable receive PMA module 40 and the programmable receive PCS module 44, may be programmed in accordance with one standard while the transmit path, i.e., the programmable transmit PCS module 42 and the programmable transmit PMA module 38, may be programmed in accordance with another standard.

[0029] Figure 3 illustrates a schematic block diagram of the programmable receive PMA module 40 that includes a programmable front-end 100, a data and clock recovery module 102, and a serial-to-parallel module 104. The programmable front-end 100, which will be described in greater detail with reference to Figures 4 - 8D, includes a tunable gain stage 108 and control module 106. The data and clock recovery module 102 includes a data detection circuit 110 and a phase locked loop 112. The phase locked loop 112 includes a phase detection module 114, a loop filter 116, a voltage controlled oscillator 118, a 1st divider module 120, and a 2nd divider module 122.

[0030] The programmable front-end 100 is operably coupled to receive the receive serial data 52 and produce amplified and equalized receive serial data 124 therefrom. To achieve this, the tunable gain stage 108 is programmed in accordance with an equalization setting 128 and an amplification setting 130, as produced by the control module 106, to provide the appropriate equalization and amplification of the received serial data 52.

[0031] The data and clock recovery circuit 102 receives the amplified and equalized receive serial data 124 via the phase detection module 114 of phase locked loop 112 and via

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programmable deserialization setting 66 provided to the programmable receive PMA module 40 by the control module 35.

[0033] The serial-to-parallel module 104, which may include an elastic store buffer, receives the recovered data 136 at a serial rate in accordance with the recovered clock 138. Based on a serial-to-parallel setting 135 and the parallel receive clock 194, the serial-to-parallel module 104 outputs the receive parallel data 54. The serial-to-parallel setting 135, which may be part of the programmable deserialization setting 66, indicates the rate and data width of the receive parallel data 54.

[0034] Figure 4 is a schematic block diagram of a programmable front-end 100 that includes control module 106 and a tunable gain stage 108. The tunable gain stage 108 includes a frequency dependent load 140 and an amplifier input section 142. The tunable gain stage 108 will be described in greater detail with reference to Figures 6 and 7.

[0035] The control module 106 generates an equalization setting 128 based on the channel response of the channel on which the receive serial data 52 is received. The control module 106 provides the equalization setting 128 to the frequency dependent load 140. The control module may also provide an amplification setting 130 to the tunable gain stage 108 based on the signal strength of the receive serial data 52.

[0036] The frequency dependent load 140, based on the equalization setting 128 and/or the amplification setting 130, adjusts its frequency response. The amplifier input section 142, in combination with the adjusted frequency dependent load 140, amplifies the received serial data 52 to produce amplified and equalized received serial data 124. Ir one embodiment, the frequency dependent load 140 includes at least one high-pass filter.

[0037] Figure 5 is an alternate schematic block diagram of a programmable front-end 100 that includes a tunable gain

stage 108 and control module 106. The tunable gain stage 108 includes 3 stages (stage 1, stage 2 and stage 3), which will be described in greater detail with reference to Figures 6 -8D, that each receive the equalization setting 128 and/or amplification setting 130 from control module 106. As shown, stage 1 receives the received serial data 52, amplifies it, equalizes it, and passes its output to stage 2 which further amplifies and equalizes the signal which passes its output to stage 3 which further amplifies and equalizes the signal to produce the amplified and equalized received serial data 124. In this embodiment, stages 1 and 2 may be considered 1st and 2nd input stages while stage 3 may be considered an output stage of the tunable gain stage 108. As one of average skill in the art will appreciate, stages 1, 2 and 3 may be individually programmed via the control module 106 and/or programmed utilizing the same equalization setting.

[0038] Figure 6 is a schematic block diagram of an embodiment of the tunable gain stage 108 of Figure 4 and/or one of the stages of the tunable gain stage of Figure 5. this embodiment, the frequency dependent load 140 includes a plurality of high-pass filters that are produced by the combination of NMOS transistors, resistors R1, R2, R3, R4 and capacitors C1, C2, C3 and C4. Note that capacitor having the designation C corresponds to the parasitic capacitance of the NMOS transistors. As one of average skill in the art will appreciate, resistors R1-R4 may be adjustable such that the frequency response of the corresponding high-pass filter may be tuned in accordance with the equalization setting. Further, the high-pass filter formed by R1, C, and C1 may be selectively enabled or disabled to further adjust the overall transfer characteristic of the frequency dependent load 140. Similarly, R4, C, and C4 may be enabled or disabled to adjust the overall transfer characteristic of the frequency dependent load 140. As one of average skill in the art will further appreciate, capacitors C1, C2, C3 and C4 may be omitted depending on the size of the parasitic capacitance C

and the desired corner frequency or frequencies of the highpass filter or filters.

[0039] The amplifier input section 142 includes a pair of NMOS input transistors that receive the received serial data 52 and are coupled to a current source. As such, the frequency dependent load 140 acts as the load for amplifier input section 142. Since the frequency dependent load 140 includes the high-pass filtering established by resistors R1-R4, capacitors C1-C4, and parasitic capacitance, the amplification of the signal also includes a filtering, or equalization, of the signal, which results in the amplified and equalized received serial data 124.

Figure 6A is a schematic block diagram of another [0040] embodiment of the tunable gain stage 108 of Figure 4 and/or one of the stages of the tunable gain stage of Figure 5. this embodiment, the frequency dependent load 140 includes a plurality of high-pass filters that are produced by the combination of NMOS transistors, resistors R5, R6, R7, R8 and capacitors C5 and C6. As shown, resistors R5 and R8 are variable resistors that are adjustable to tune the corresponding RC high pass filter (i.e., the high pass filter produced by the resistor, e.g., R5 (or R8) and the associated capacitor, e.g., C5 (or C6)) to obtain the desired corner frequency. Further, resistors R6 and R7 provide loading for the amplifier such that the output impedance, voltage levels, and/or power levels of the gain stage are at desired values. In yet another embodiment, C5 and C6 are the parasitic capacitances of their associated transistors.

[0041] The amplifier input section 142 includes a pair of NMOS input transistors that receive the received serial data 52 and are coupled to a current source. As such, the frequency dependent load 140 acts as the load for amplifier input section 142. Since the frequency dependent load 140 includes the high-pass filtering established by resistors R5 and R8 and the capacitors C5 and C6, the amplification of the signal also includes a filtering, or equalization, of the

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                                                                                                                            the trequency dependent load law includes resistors and its map amount capacitors c1 and c2. IMMOS transistors map amount capacitors c1 and c2. IMMOS transistors map amount capacitors capacitant rarea it in capacitant ca
                                                                                                                                                             corresponding parasitic capacitance transistor and current transistor transistor
                                                      serial data 124.
                                                                                                                                                                          input section 142 includes an input transistor and current and input transistor and current and input section 142 and the amplifier input section race the race and amplifier and amplif
                                                                                                                                                                                          source. In combination, the amplifier input section 142 and the amplifier input section 142 and received the received and equalizes the received and equalizes and equalizes and emialized and emializ
                                                                                                                                                 corresponding parasitic capacitance (Co).
                                                                                                                                                                                                               trequency dependent produce the amplified and equalized to produce the amplified and serial data 152 to produce the amplified and received earial data 171
                                                                                                                                                                                                                                                                                                                                                                                                            serial coata 144. skill in the art will appreciate;

As one of average skill in the art will appreciate;

As one of average 1/10 chown in a cho
                                                                                                                                                                                                                                                             the frequency dependent load 140 shown in Figures 6 and/or 7 or emalizations to new include more or less high-nass filtering or emalization and include time the high-nass filtering or emalization.
                                                                                                                                                                                                                                                                                            may include more or less resistor-capacitor combinations to the high-pass filtering, or equalization, the resistors filtering 
                                                                                                                                                                                                                                                                                                         further fine tune the high-pass filtering, or equalization, the resistors further, the high-pass filtering, or equalization, the resistors further, the high-pass filtering, or equalization, the resistors analyzed further fine tunable gain stage.

And or canacitors may be additionable and individually provided by the tunable and or canacitors may be additionable and or equalization.
                                                                                                                                                                                                                                                                                                                              provided by the tunable gain stage. Further, the resistors and individually enabled en
                                                                                                                                                                                                                                   received serial data 124.
                                                                                                                                                                                                                                                                                                                                                and/or capacitors may be adjustable and individually enal and/or equalization, and/or equalization, to adjust the high-pass rain erams in the runable main erams in the runable main erams.
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The strength of a change of a chang
                                                                                                                                                                                                                                                                                                                                                                                                              between two programmable logic devices 10. As shown, the transmission line and a 3th transmission connector and a 3th transmission channel includes a line a 2th connector and a 3th transmission channel a 2th transmission line.
                                                                                                                                                                                                                                                                                                                                                                provided by the tunable gain stage 108.
                                                                                                                                                                                                                                                                                                                                                                                                                              channel includes a transmission line (TX line), a connector, transmission line (TX line), a connector, transmission line (TX line), a connector, and a 3<sup>rd</sup> transmission line, a 2<sup>rd</sup> connector and a 3<sup>rd</sup> transmission line, a 2<sup>rd</sup> transmission line, a 2<sup>rd</sup> transmission line, a 2<sup>rd</sup> transmission line.
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          ransmission line, a 2 connector and a 3 transmission circuits and a a connector and a a transmission represent the printer where the printer where the printer of the configuration is typical hoards where the printer of the configuration are remarked to the configuration as a fearant printer of the configuration and a second configuration as a configuration as a configuration of the configuration and a second configuration and a second configuration as a configuration and a second configuration are configuration.
                                                                                                                                                                                                                                                                                                                                                                                                                                                             line. This configuration is typical for integrated circuits on is typical for integrated the printed on different printed circuit boards where this mounted on different printed ria a harmane mounted on arras are commissioned ria a harmane circuit hoards are commissioned ria a harmane mounted on arras are commissioned to the circuit hoards are commissioned to the circuit hoards are commissioned to the printed the printed to the printed to
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 circuit boards are coupled via a backplane, be up to a rhe circuit boards the integrated high-speed serial dara configuration, distance for high-speed serial anart
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 configuration, the integrated high-speed serial annrows; and remire and remire and remire apart.
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  mounted on altrerent princed via a backplane.
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              apart. At this distance, for high-speed serial data, the appropriate significant and require appropriate channel response will be significant and require appropriate
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             10n. Figure 8B illustrates a channel that includes a
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               rigure 8B illustrates a channel that includes a logic devices a channel that logic devices a channel that logic devices a channel that includes a representation that logic devices a channel that logic devices a channel that includes a result in that logic devices a channel that includes a result in that includes a representation of the same programmable logic devices a channel that includes a representation of the same programmable logic devices a channel that includes a representation of the same programmable logic devices a channel that includes a representation of the same programmable logic devices a channel that includes a representation of the same programmable logic devices are representation of 
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10 that may be on the same printed circuit board.
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             equalization.
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of Figure 8A. As such, its channel response will have less adverse affects on high-speed data than the channel of Figure 8A.

[0046] Figure 8C illustrates the channel response for the channels of Figures 8A and 8B. As shown, the channel for Figure 8A has a corner frequency that occurs at a frequency lower than the channel response for the channel of Figure 8B. In addition, the attenuation rate may be greater for the channel of Figure 8A than for Figure 8B. In addition, Figure 8C illustrates the data transmission rates that may traverse the channels of Figures 8A and 8B. As shown, a 3.125 gigabits-per-second transmission rate occurs at a lower frequency than 6.25 gigabits-per-second, which, in turn, is less than the 10 gigabits-per-second.

[0047] As is further shown for the 3.125 gigabits-persecond rate, the channel response for the channel of Figure 8B has minimal effect on the data being transmitted while the channel of Figure 8A begins to attenuate the data transmissions at the 3.125 gigabits-per-second rate. As is known, attenuation distorts the signals and thus reduces the receiver's sensitivity. As further shown, the 6.25 gigabits-per-second rate is significantly attenuated by the channel of Figure 8A and is somewhat attenuated by the channel of Figure 8B. The 10 gigabits-per-second rate is significantly attenuated by either channel.

[0048] Figure 8D illustrates the programmable equalization provided by the programmable analog front-end of the present invention. As shown, the equalization for 3.125 gigabits-per-second rate may be set to compensate for the channel response of Figures 8A or 8B. As the transmission rate increases and/or the channel response increases (i.e., the channel length increases), the amount of attenuation increases thus requiring the equalization to increase. As shown, the programmed equalization is significantly greater for 6.25 gigabits-per-second than it was for 3.125 gigabits-per-second and is even greater for 10 gigabits-per-second.

[0049] The preceding discussion has presented a programmable analog front-end that includes built-in equalization. By tuning the equalization within the analog front-end, the channel response for various channels may be more appropriately compensated thus improving the receiver sensitivity, which in turn increases the reliability of high speed data transmissions. As one of average skill in the art will appreciate, other embodiments may be derived from the teaching of the present invention without deviating from the scope of the claims.